

# A45D01

## TABLE OF CONTENTS

COVER SHEET	1
BLOCK DIAGRAM	2
POWER DELIVERY CHART	3
CLOCK DISTRIBUTION	4
MISC TABLE	5
FT1 PCIE/UMI	6
FT1 DDR3 MEM I/F	7
FT1 DISPLAY & MISC	8
FT1 POWER & GND	9
DDR3 DIMM-1	10
DDR3 DIMM-2	11
FCH-PCIE/PCI/APU/LPC/CLK	12
FCH-ACPI/GPIO/USB/PHY/AZ	13
FCH-SATA/HWM/SPI	14
FCH-POWER & DECOUPLING	15
FCH-STRAPS	16
Scaler	17
CRT translator LVDS	18
Reserved	19
REAR USB CONN & PS/2	20
FRONT USB HEADER	21
LAN RTL8111E	22
LAN CONN & USBX2	23
ALC887VD	24
AUDIO CONNECTOR	25
CIR & HWM	26
SERIAL PORT HEADER & TPM	27
APU FT1 VCORE POWER	28
APU FT1 1D05V/1D8V	29
DDR3 MEMORY POWER	30
1D1V / FCH 1D1V POWER	31
Mini PCIe slot	32
STANDBY POWER & 12V POWRR	33
ATX CONN & FRONT PANEL	34
FANS & PWRGD & ENABLES	35
USB3.0	36
Card Reader	37
SIO IT8728F_CX	38
LPT & COM	39
Power Plane/3D3V_SB	40
ISL62392C_5V_S5/3D3V_S5	41

## FAB 1.0

### PCB SIZE:

9.1" X 7.5" 4 layers PCB

### CPU:

AMD BROZAS APU FT1 19mm x 19mm, 0.8mm pitch BGA 413 BALL

### System Chipset:

FCH Hudson-D1 A13 23mm x 23mm 0.8 mm Pitch FCBGA 605-BALL

### Main Memory:

SINGLE Channel / DDR-III \* 2 (Max 8GB)

### On Board Device:

VRD(Type): Intersil ISL6265

LAN: RealTek 8111E

HDA Codec: ALC887


BIOS: SPI Flash ROM 1M Byte

Super IO: ITE8728F CX

### Expansion Slots:

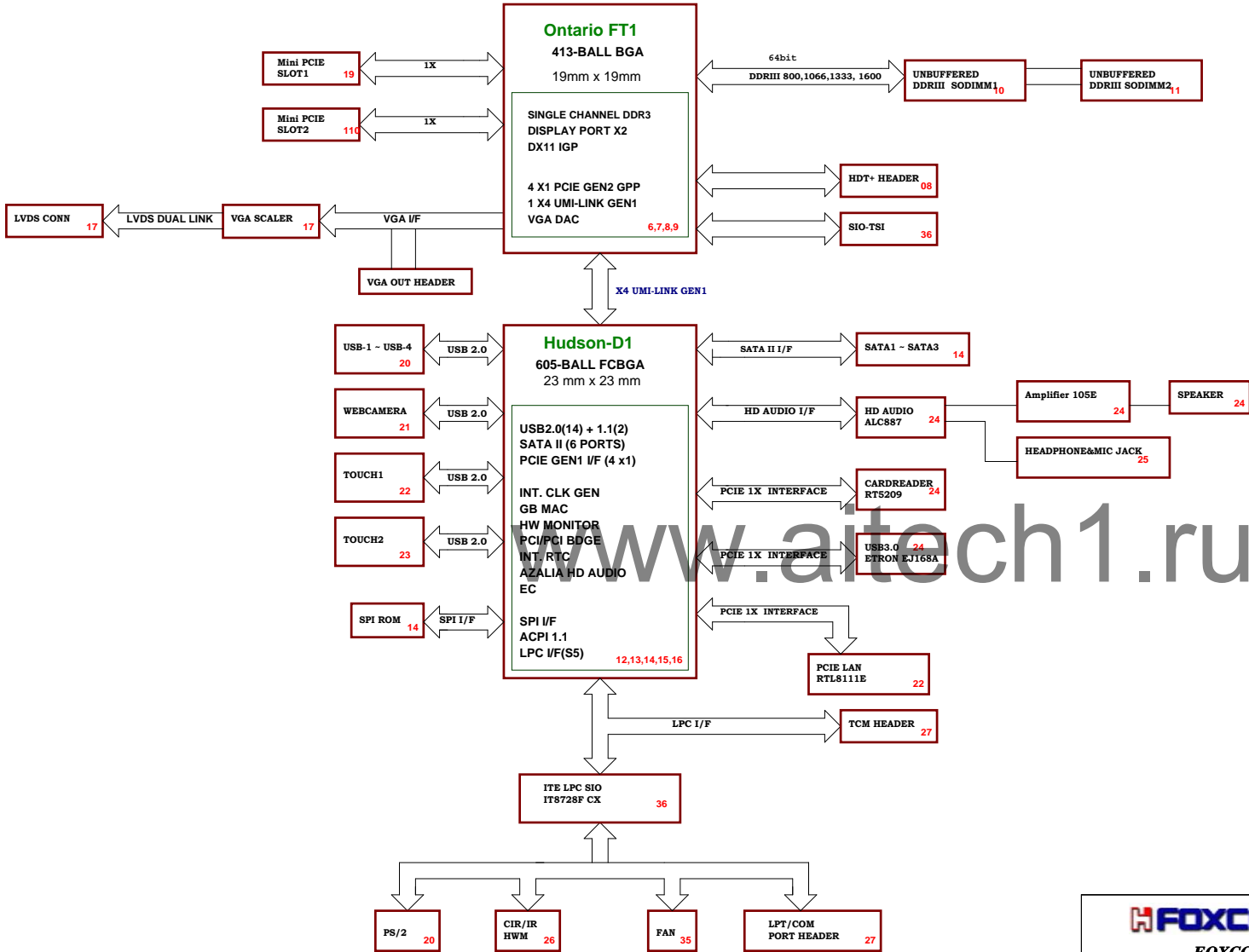
Mini PCI-E SLOT \*2

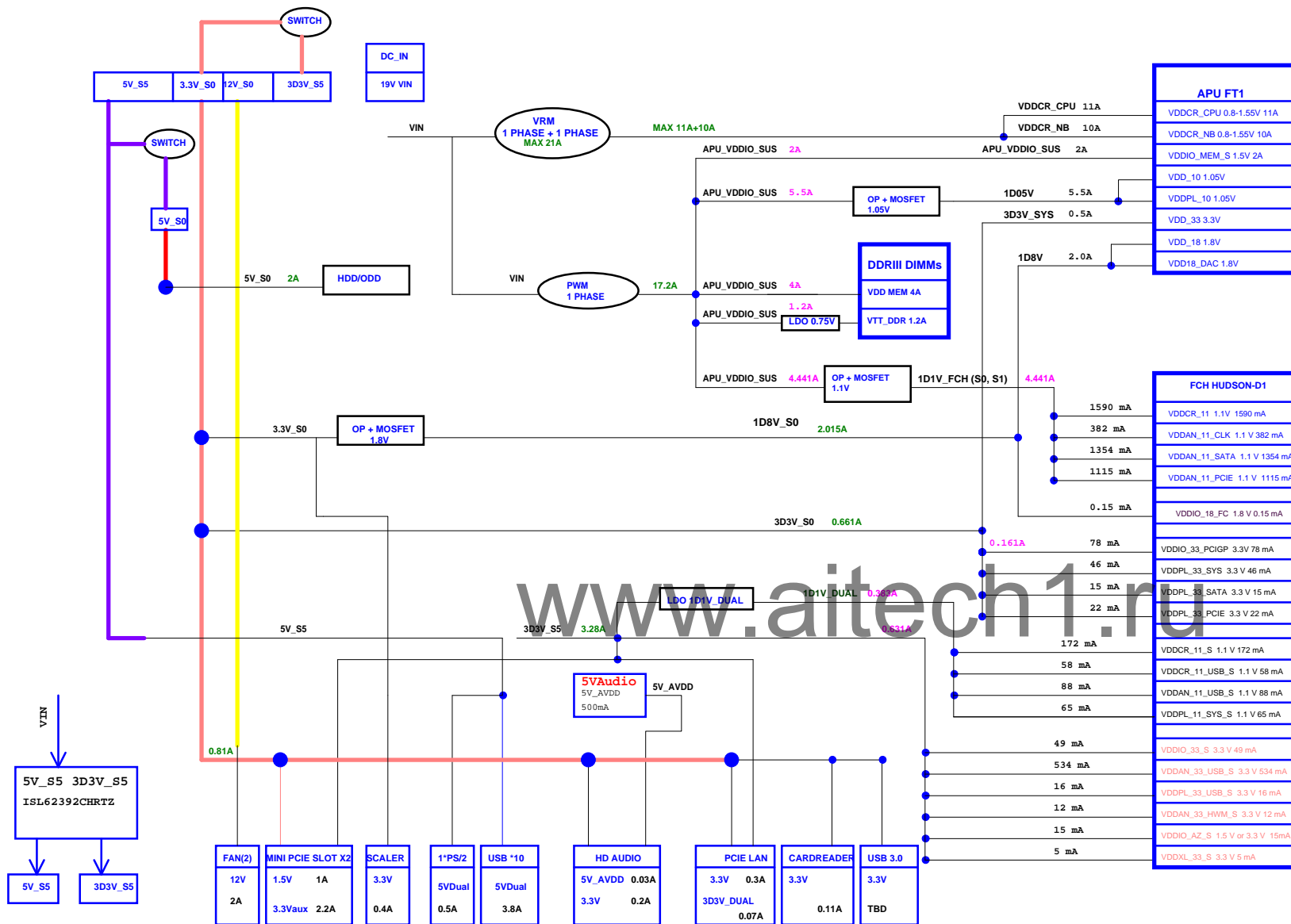
Version	Function	SKU	BOM
Fab.A			
Fab.B			

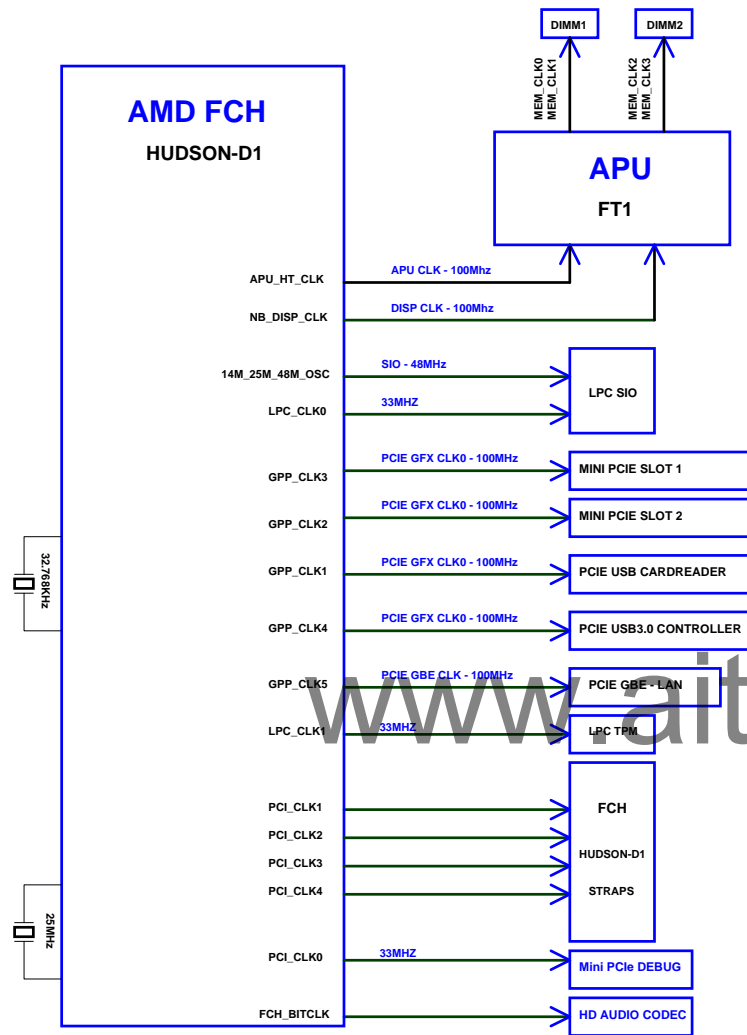
	
TABLE OF CONTENTS	
Size	Document Number
Custom	A45D01
Date: Saturday, November 19, 2011 Sheet 1 of 41	

A45D01 BLOCK DIAGRAM

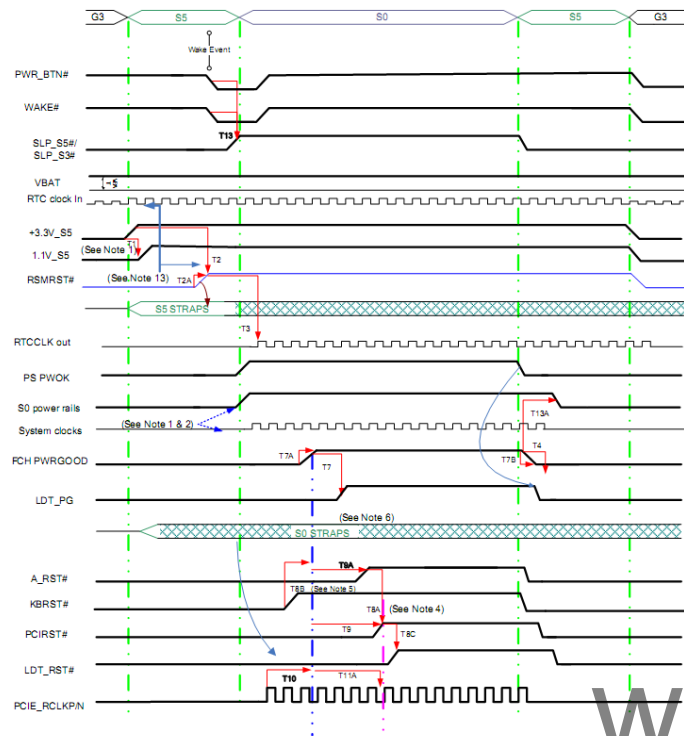
AMD FUSION APU FT1+Hudson-D1



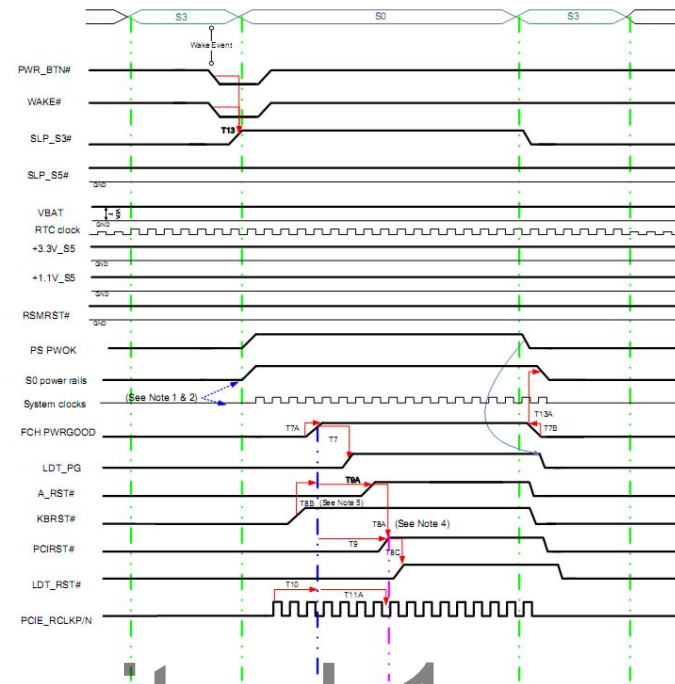




## Power sequence



**Figure 14. Power-on Sequence (S5 → S0 → S5)**

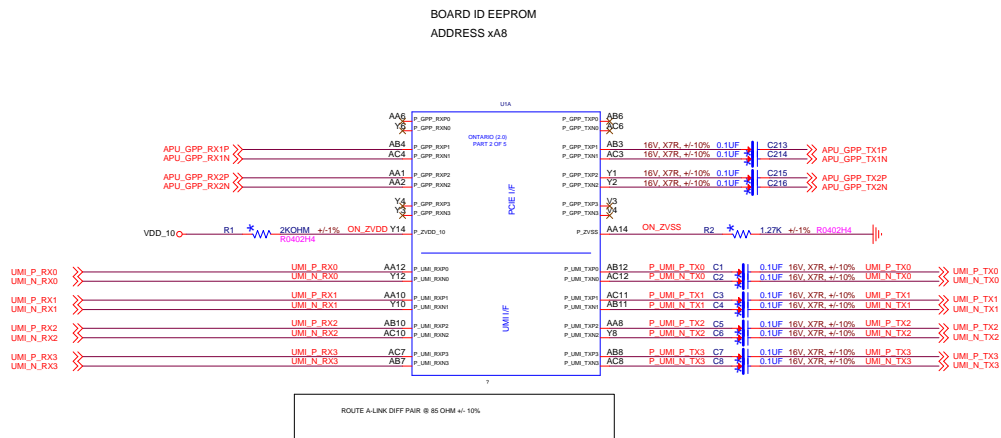


**Figure 15. Power-on Sequence (S3 → S0 → S3)**

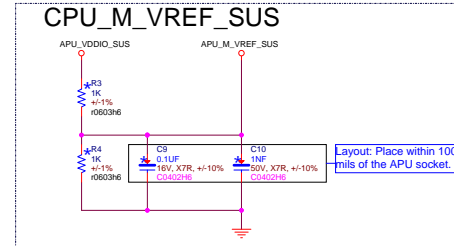
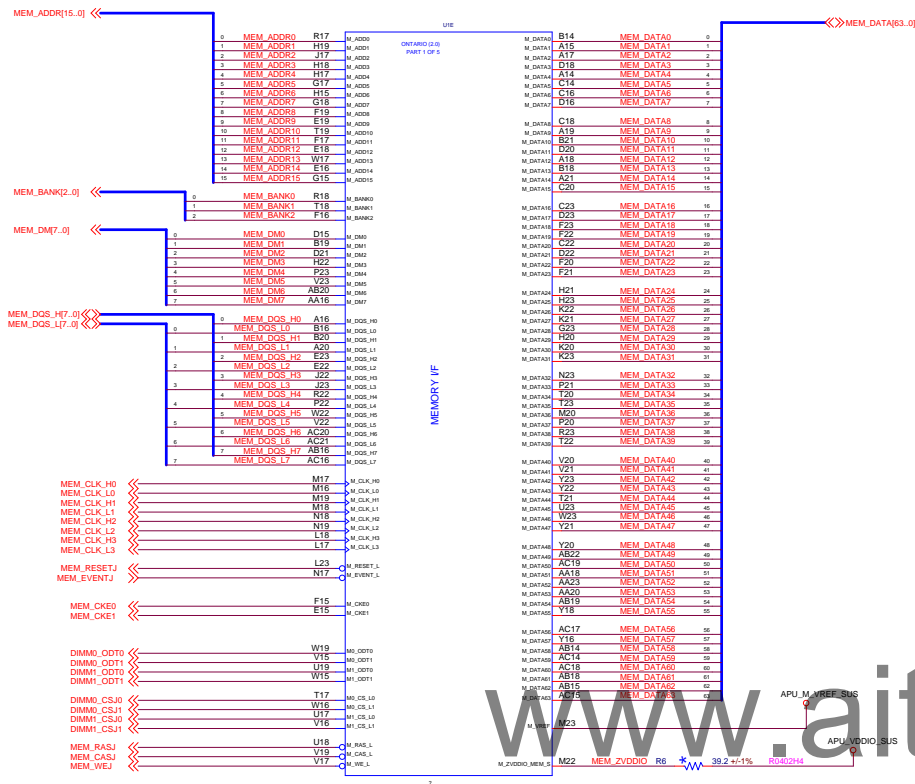
POWER RAIL		S0	S1	S3	S4	S5
5V_SB	+5V	ON	ON	ON	ON	ON
5V_DUAL	+5V	ON	ON	ON	ON	ON
30DV_DUAL	+3.3V	ON	ON	ON	ON	ON
1VBAT	+3.0V	ON	ON	ON	ON	ON
10DV_DUAL	+1.1V	ON	ON	ON	ON	ON
+12V	+12V	ON	ON	OFF	OFF	OFF
-12V	-12V	ON	ON	OFF	OFF	OFF
5V_SYS	+5V	ON	ON	OFF	OFF	OFF
30DV_SYS	+3.3V	ON	ON	OFF	OFF	OFF
5V_AVDIO	+5V	ON	ON	OFF	OFF	OFF
18RV	+1.8V	ON	ON	OFF	OFF	OFF
10DV_FCH	+1.1V	ON	ON	OFF	OFF	OFF
VDDCR_CPU	SV1	ON	ON	OFF	OFF	OFF
VDDCR_NBS	SV1	ON	ON	OFF	OFF	OFF
APU_VDDIO_SUS	+1.5V	ON	ON	ON	OFF	OFF
APU_VTT_SUS	+0.75V	ON	ON	OFF	OFF	OFF

DEFAULT JUMPER SETTING FOR POWER ON		
JUMPER	DEF.	FUNCTION

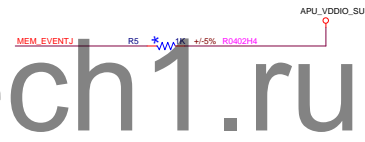
				
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Title				
<b>MISC TABLE</b>				
Size	Document Number			
Custom	<b>A45D01</b>			
Date:	Wednesday, October 26, 2011	Sheet	5	of 41

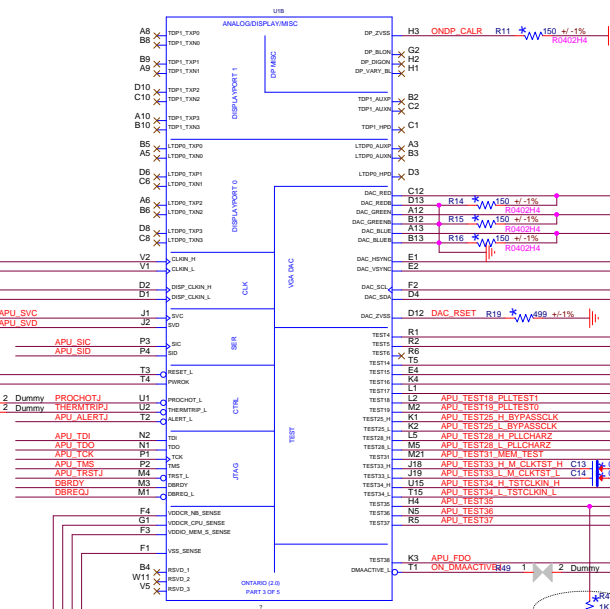
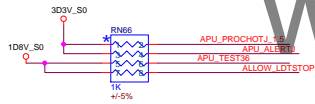
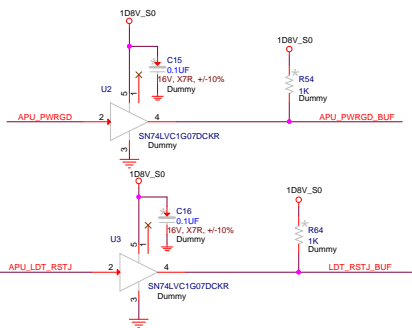
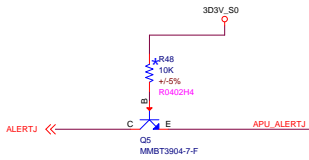
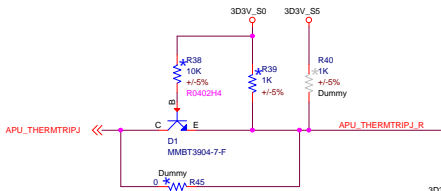
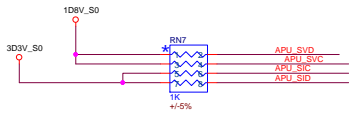
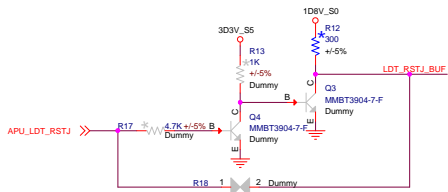
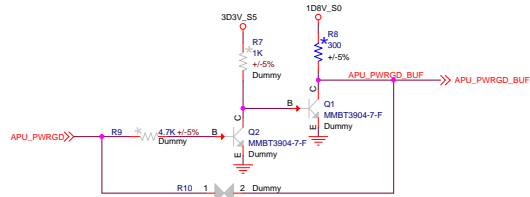


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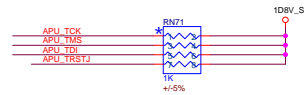
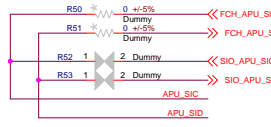
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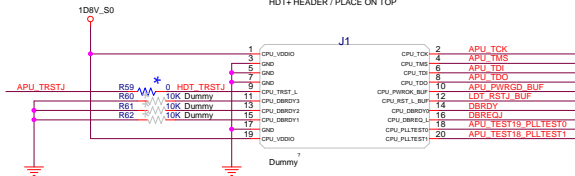


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#### DIFFERENTIAL ROUTING



#### HDT+ HEADER / PLACE ON TOP



File	FT11 DISPLAY & MISC
Size	Document Number
Customer	A45D01
Date	Wednesday, October 26, 2011
Sheet	8 of 41

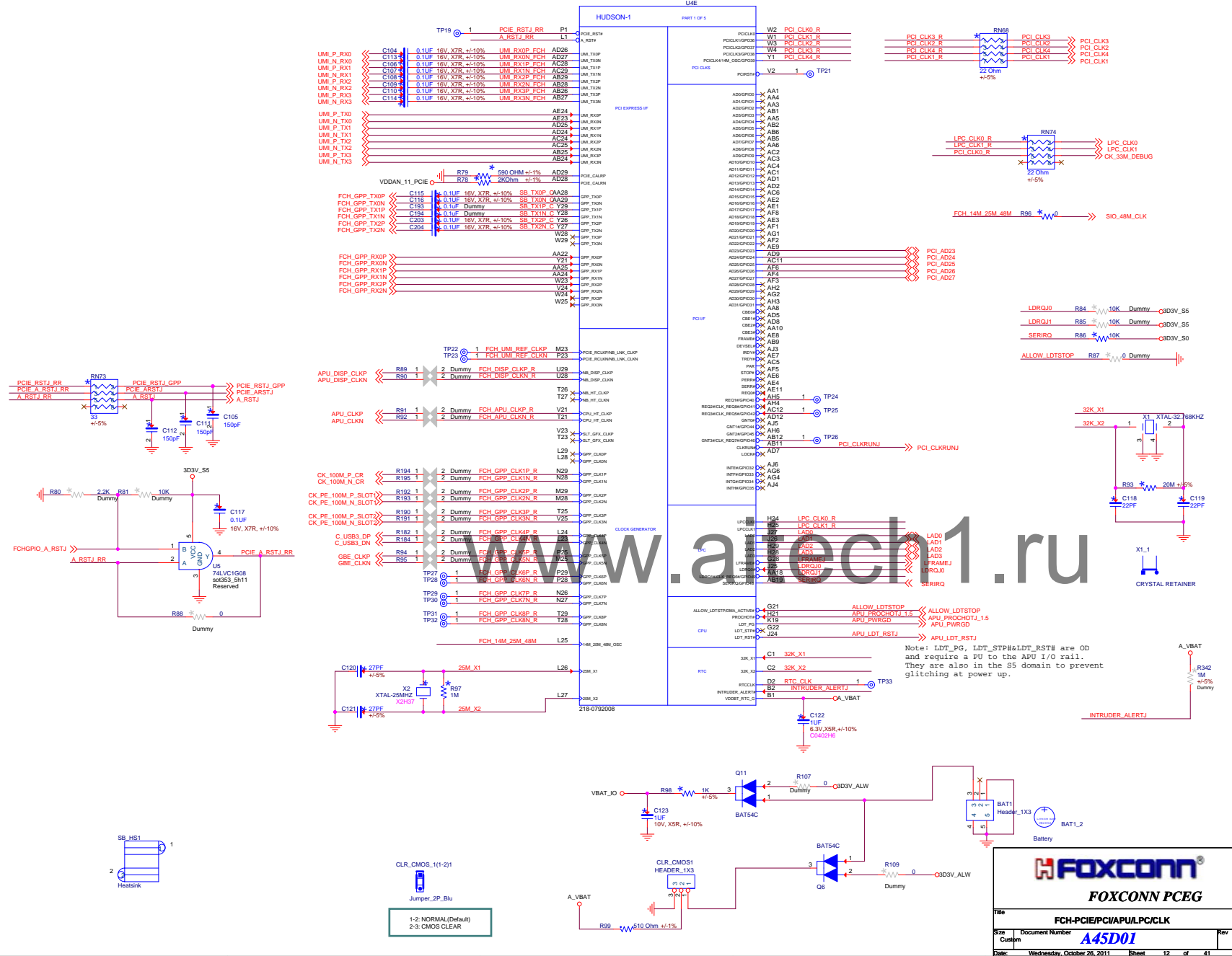


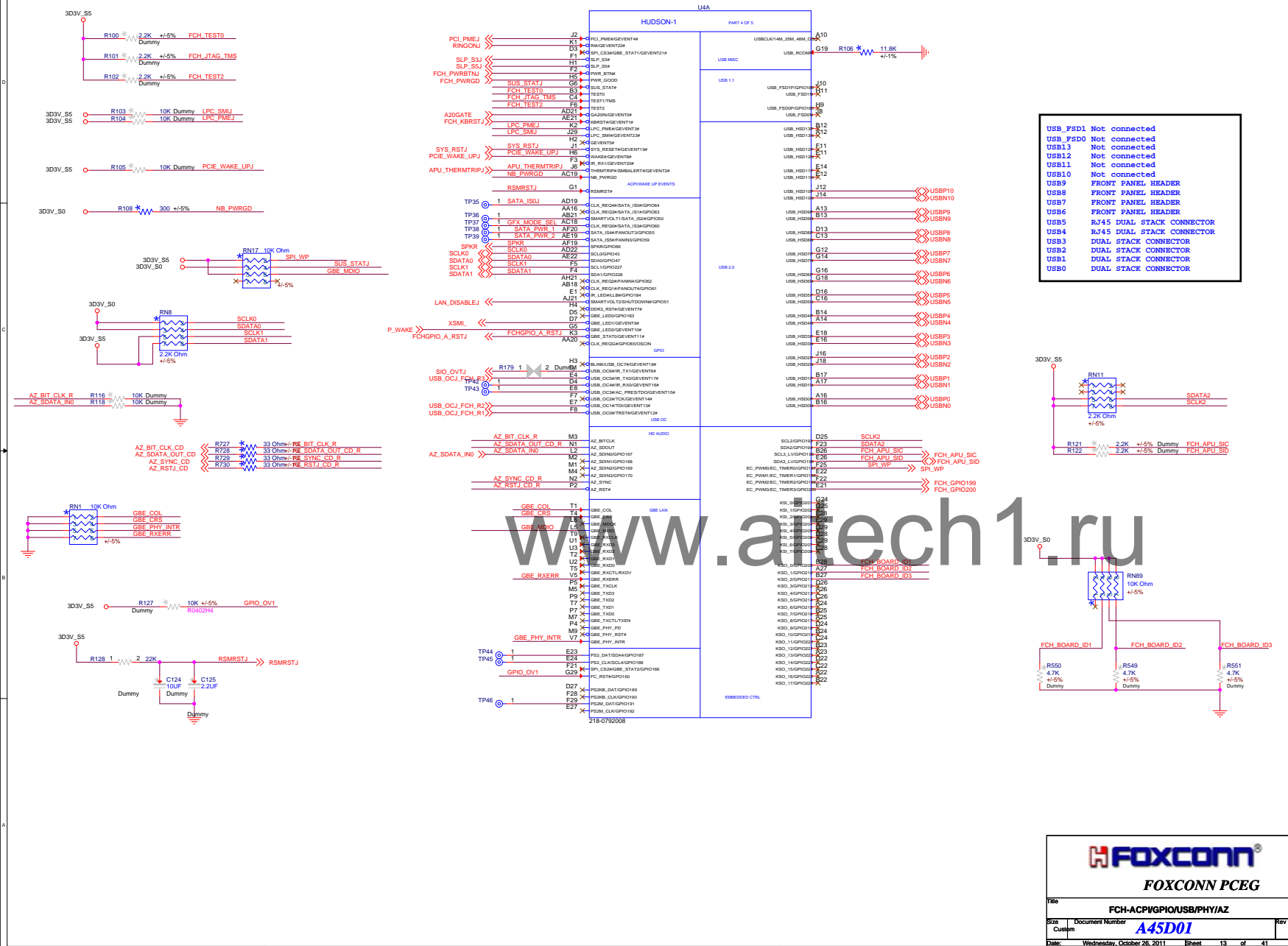




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<b>FOXCONN PCEG</b>		
Title		
DDR3 DIMM-2		
Size	Document Number	Rev
Custom	<b>A45D01</b>	
Date: Wednesday, October 26, 2011 Sheet 11 of 41		

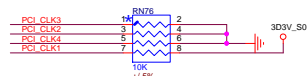
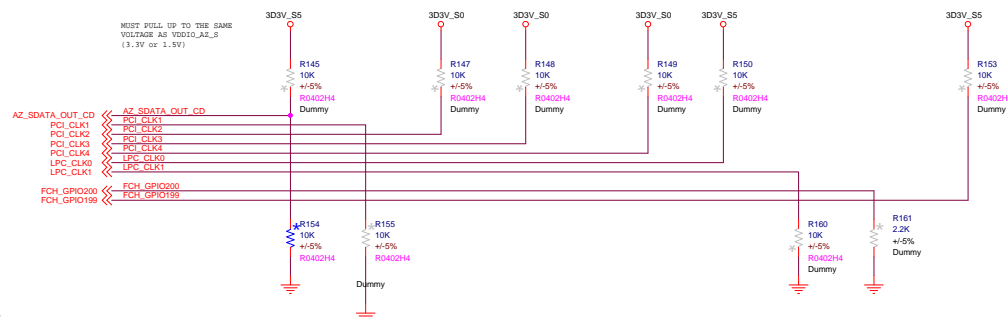






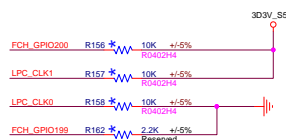


# FCH REQUIRED STRAPS



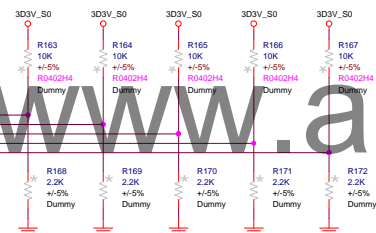
	AS_S00T	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIe GEN2	WATCHDOG TIMER ON HW_PWRD ENBLD	USE DEBUG STRAPS	NON-FUSION APU CLOCK MODE	EC ENABLED	CLAGEN ENABLED	ROM TYPE: N, N = Reserved	
<b>PULL LOW</b>	HIGH PERFORMANCE MODE	FORCE PCIe GEN1	WATCHDOG TIMER ON HW_PWRD DISABLED	IGNORE DEBUG STRAPS	FUSION APU CLOCK MODE	EC DISABLED	CLAGEN DISABLED	N, L = SPI ROM L, N = LPC ROM L, L = PWR ROM	DEFAULT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		

HUDSON-D1 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]



## FCH DEBUG STRAPS

PCI\_AD27  
PCI\_AD26  
PCI\_AD25  
PCI\_AD24  
PCI\_AD23

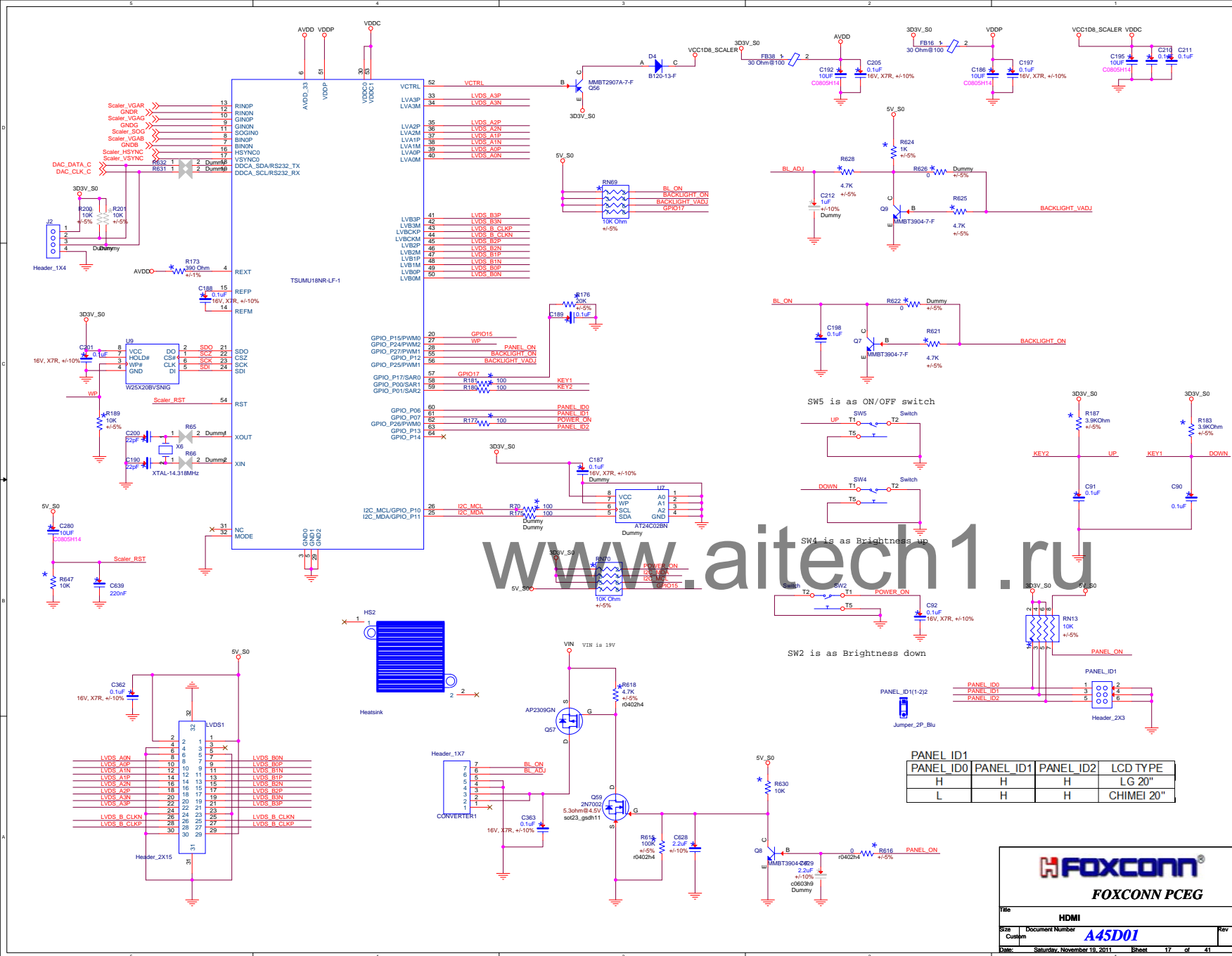


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE PC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEN BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS PC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEN BOOT

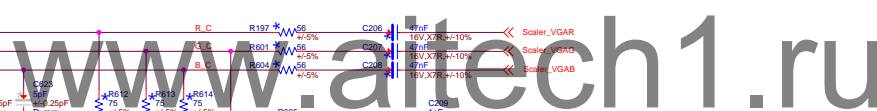


File	FCH-STRAPS	
Size	Document Number	Rev
Custom	A45D01	B
Date	Wednesday, October 26, 2011 Sheet 16 of 41	





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*FOXCONN PCEG*

Title		
PCIE x16 CONNECTOR		
Size A	Document Number <i>A45D01</i>	Rev
Date:	Wednesday, October 26, 2011	Sheet 19 of 41



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***FOXCONN PCEG***

Title

**FRONT USB HEADER**

Size  
A

Document Number

***A45D01***

Rev

Date:

Wednesday, October 26, 2011

Sheet

21

of

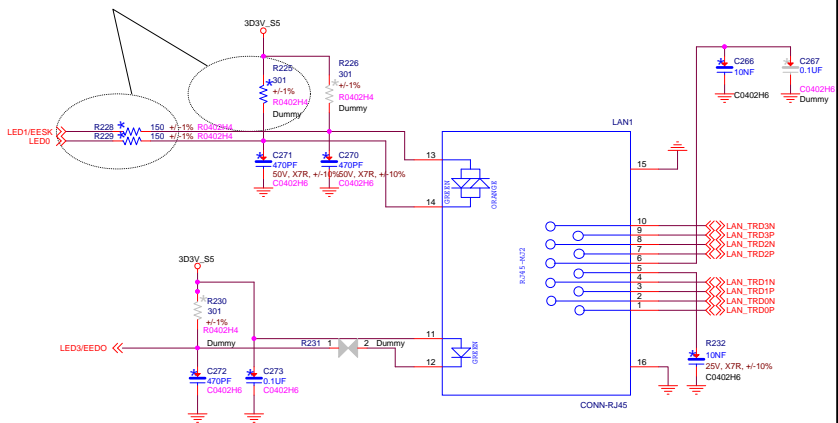
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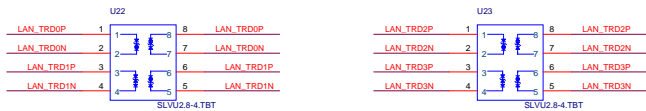
## LAN CONN

For RTL8105E LED:  
Install R307, Dummy R309  
---Modify by Dirk 2010-11-09

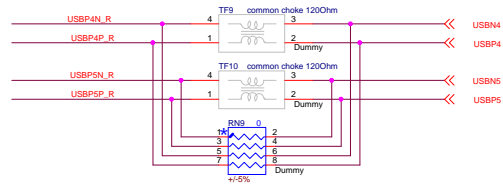
OFF = LINK 10 Mbps  
GREEN = LINK 100 Mbps  
YELLOW = LINK 1000 Mbps



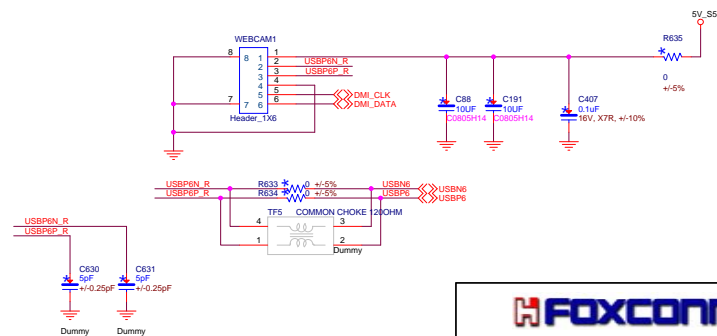
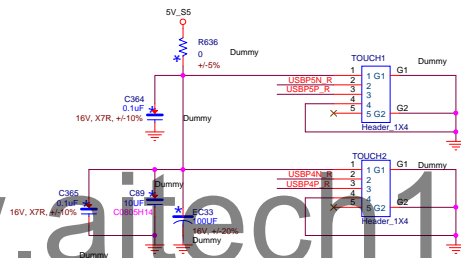
ACTIVE LED  
GREEN = LINK UP  
BLINKING = TX/RX ACTIVITY



## USB Device

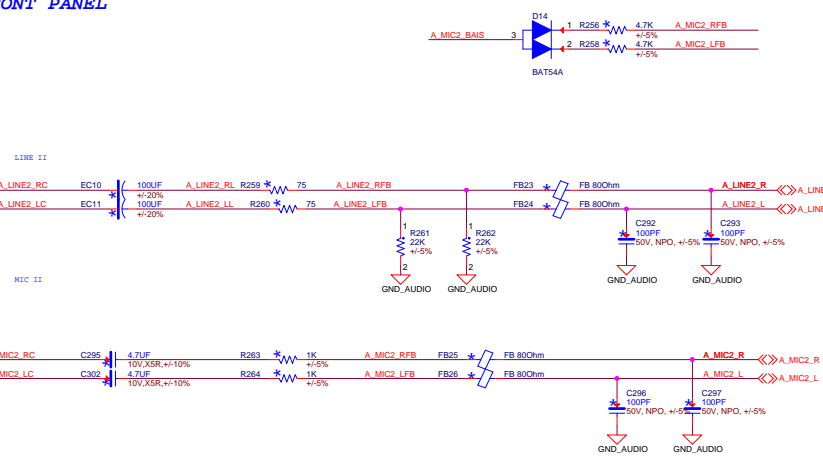
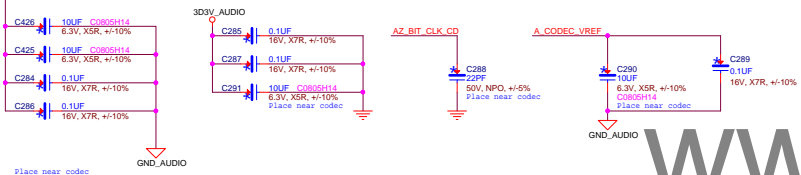


two common chokes and RESA co-layout



**FOXCONN PCEG**

Title			
LAN CONN & USBX2			
Size	Document Number	Rev	
Custom	A45D01		
Date:	Wednesday, October 26, 2011	Sheet	23 of 41



All of JD resistors should be placed as close to the codec sense pin.

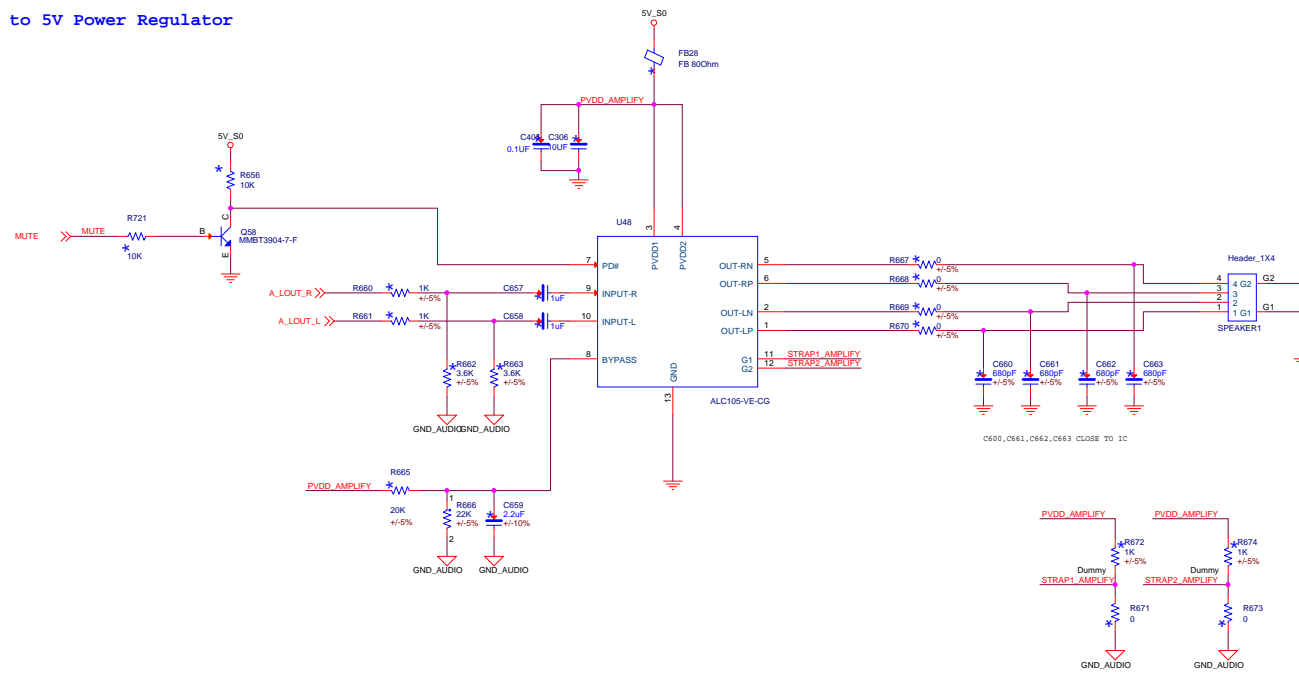
The screenshot displays a web browser window with the address bar showing the URL `www.aitech1.ru`. Below the browser, a network packet capture interface is visible, showing a packet from `A_SENSE` to `A_LINE_ID` with a payload of `39.2K` and a status of `+1%`. The packet capture interface also shows a packet from `codec.sense.pin` to `codec.sense.pin`.



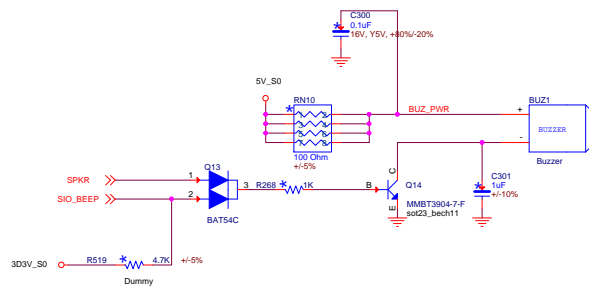
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ALC662			
Size	Document Number		Rev
Custom	A45D01		
Date:	Wednesday, October 26, 2011	Sheet	24 of 41



## 12V to 5V Power Regulator

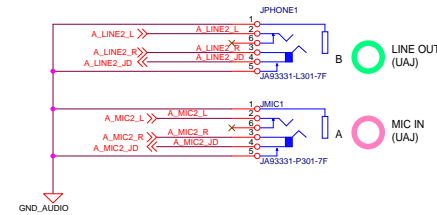


## BUZZER/Speaker Header



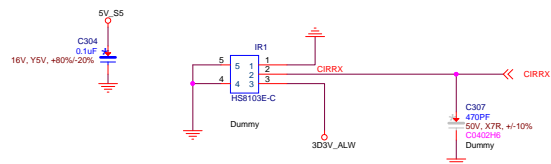
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## Audio CONN (3 Port)



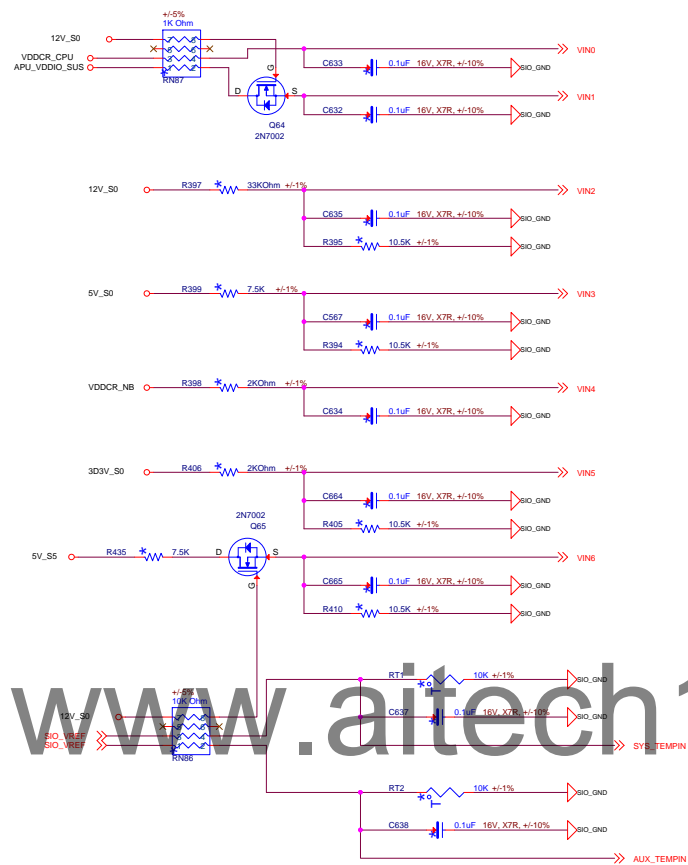
<b>FOXCONN</b> FOXCONN PCEG	
File	
AUDIO CONNECTOR	
Size	Document Number
Custom	<b>A45D01</b>
Date	Wednesday, October 26, 2011 Sheet 25 of 41

## IR/CIR



IR/CIR CONNECTOR

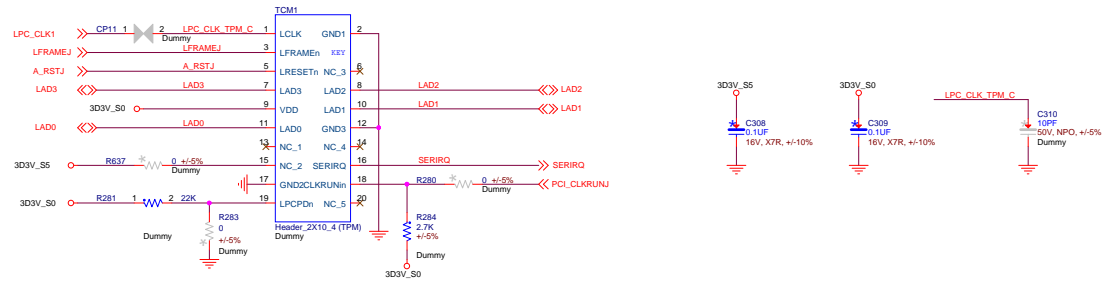
## POWER RAILS MONITOR



**FOXCONN PCEG**

Title			
CIR & HWM			
Size	Document Number		Rev
Custom	A45D01		
Date:	Wednesday, October 26, 2011	Sheet	26 of 41

TPM



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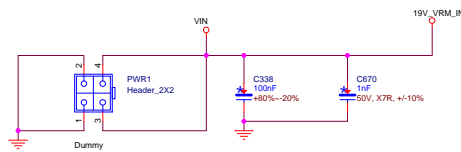
### Metal VID Codes

### VFIXEN VID Codes

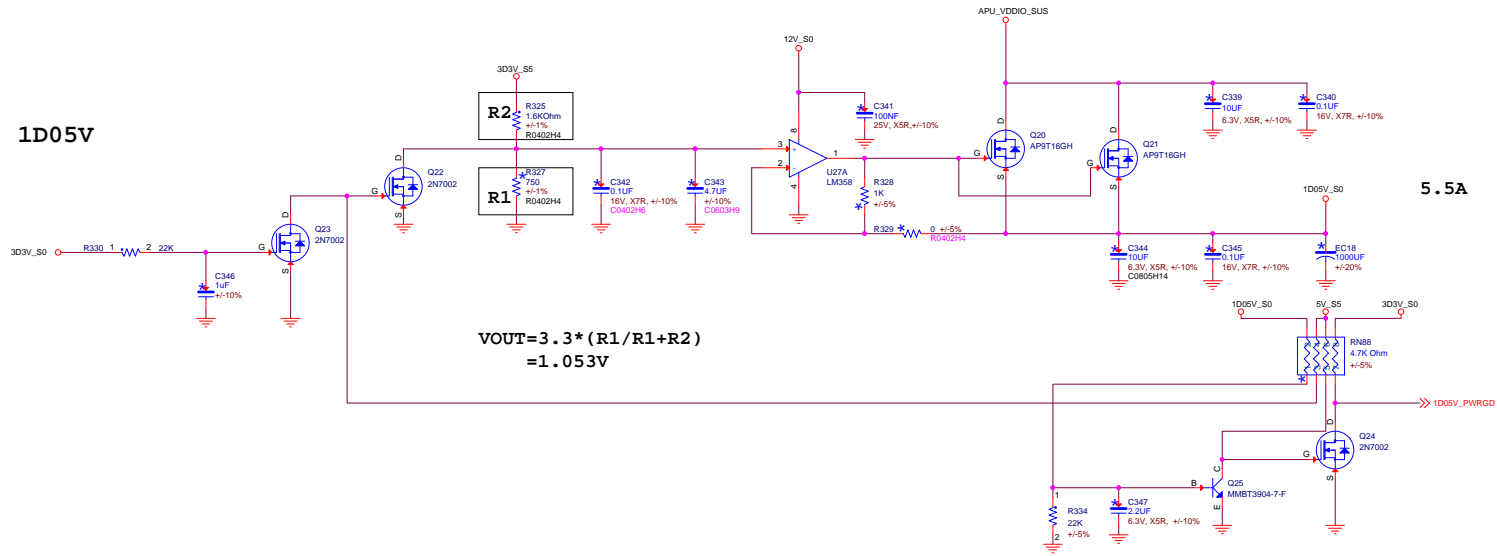
```

change VRM_PWRGD pull high from 3D3V_DUAL to 3D3V_SYS,
adjust VRM_PWRGD output rise and fall pulse)
Modify by dirk 2010-11-01

```

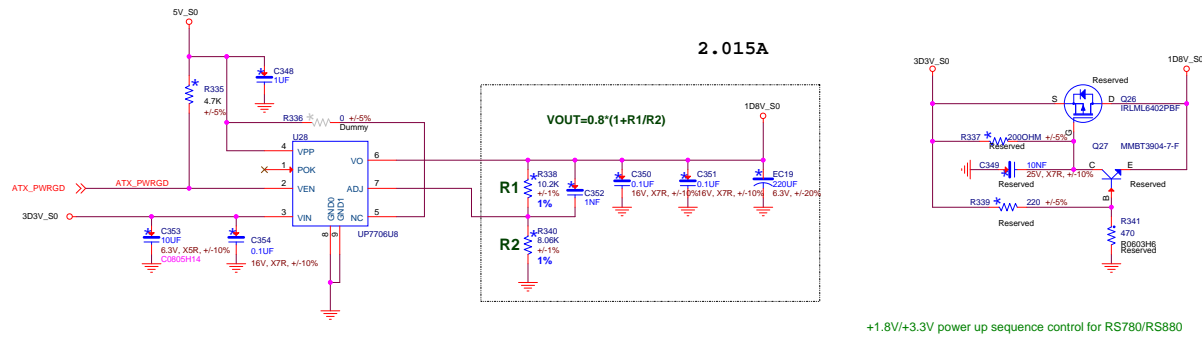


1D05V

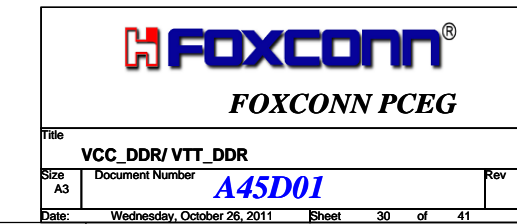
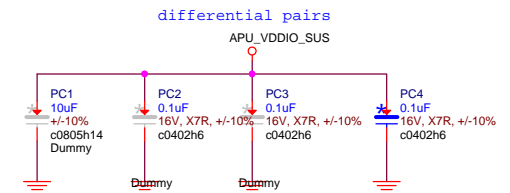


1D8V

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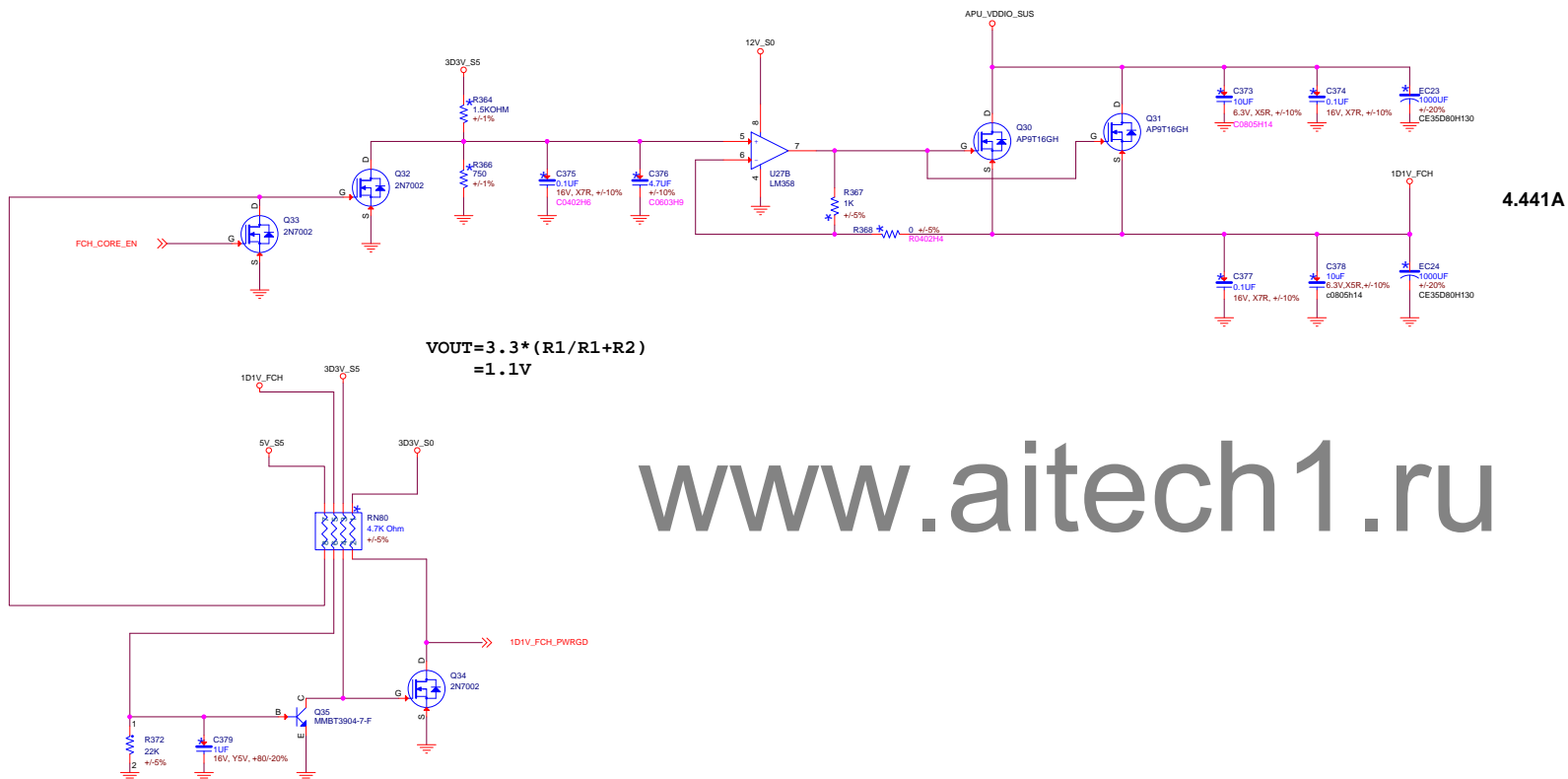


**VTT\_DDR**



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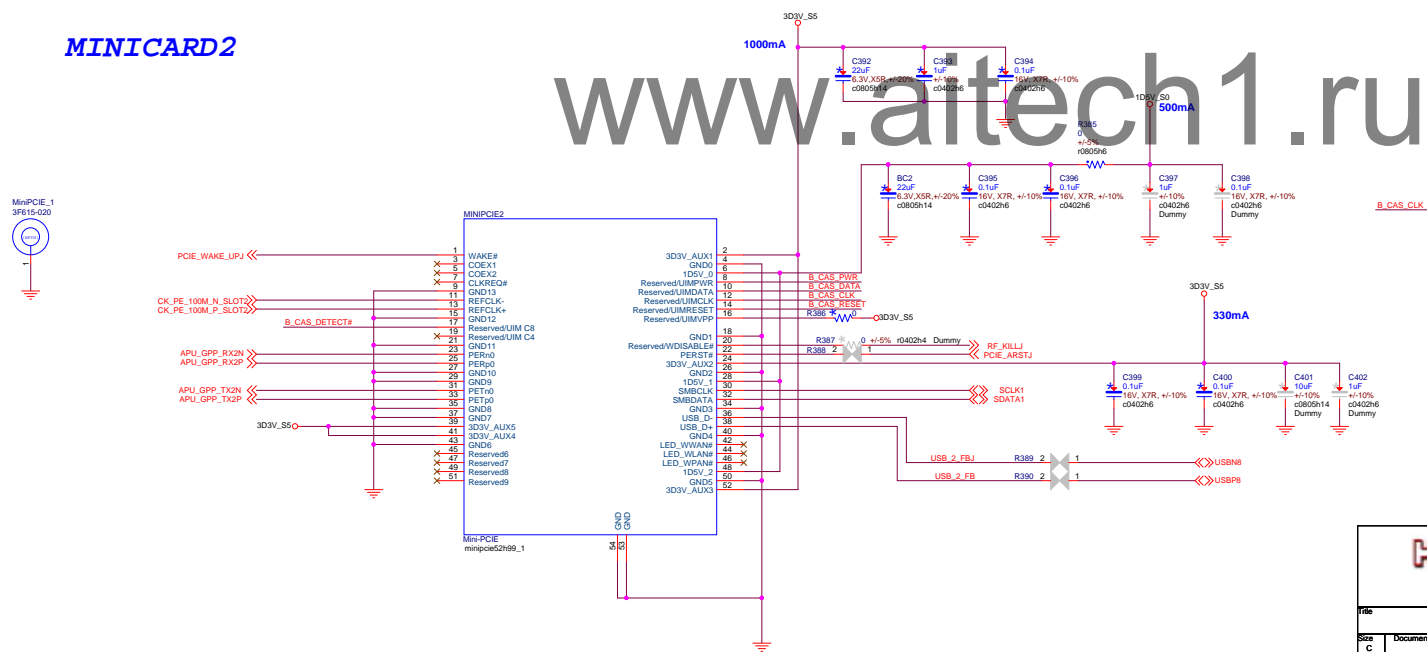
1D1V\_FCH



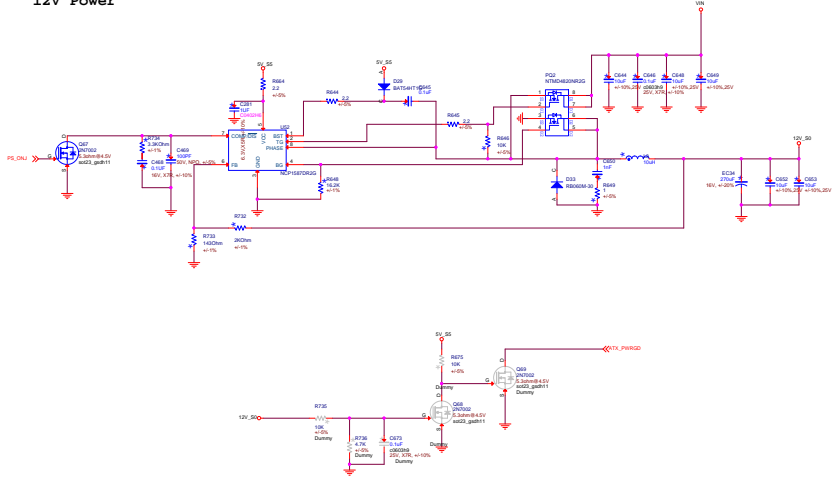
[www.aitech1.ru](http://www.aitech1.ru)



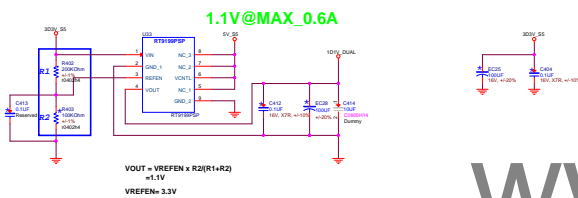
## MINICARD2



## 12V Power

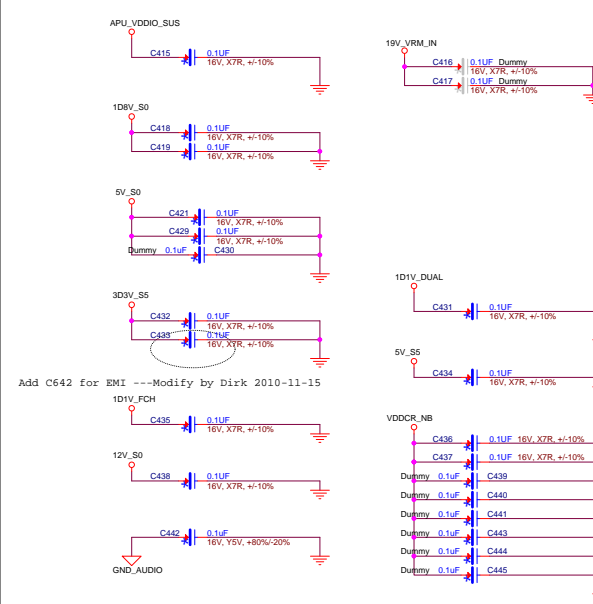
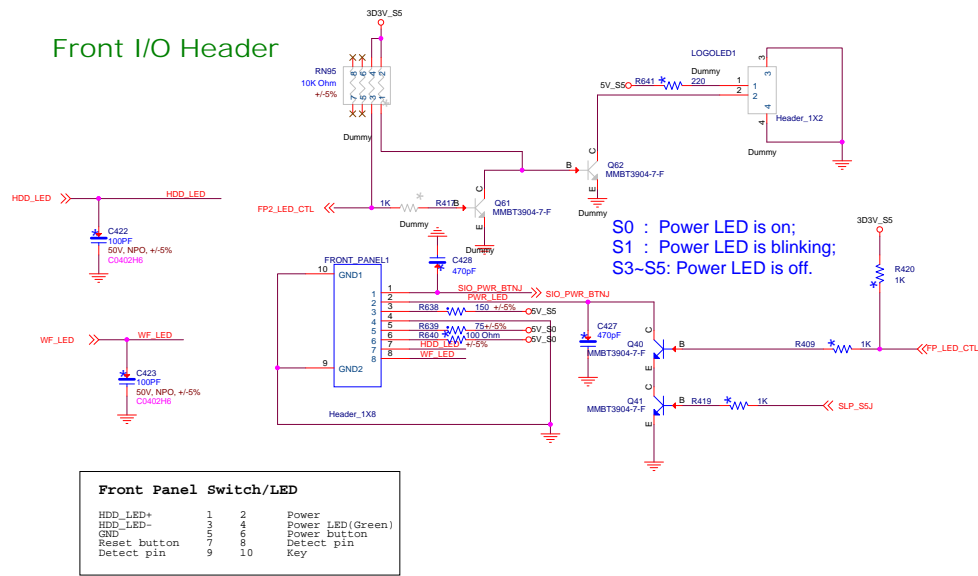


## 1D1V EUP

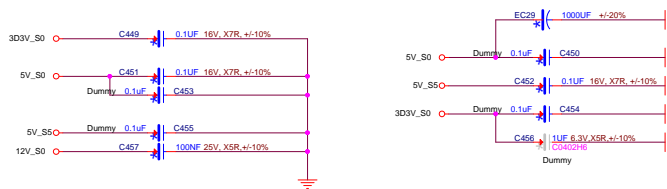


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## Front I/O Header

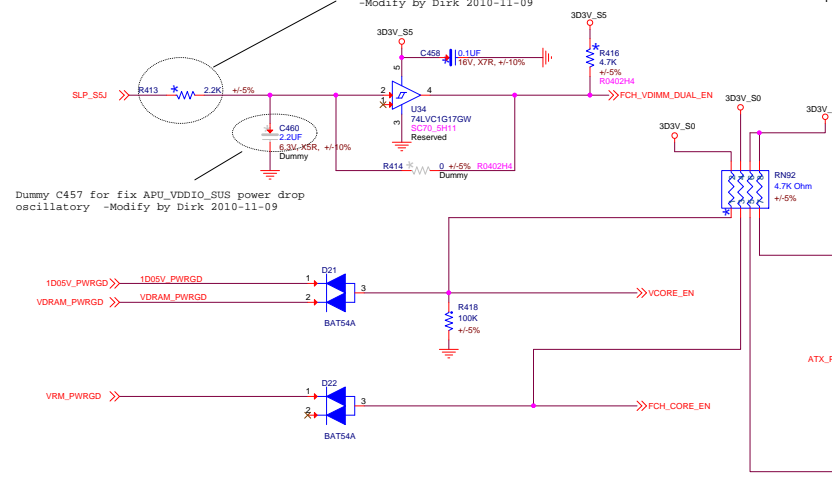


## ATX POWER CONN



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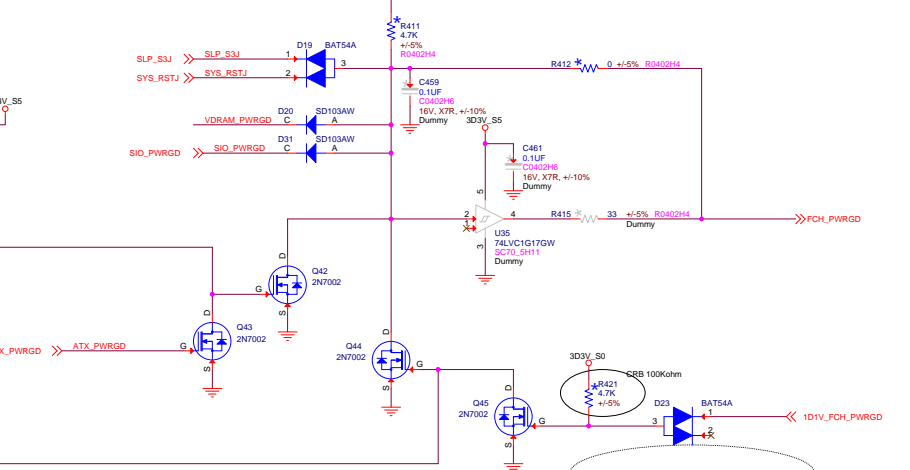
POWER GOOD & ENABLES CIRCUIT



Dummy C457 for fix APU\_VDDIO\_SUS power drop oscillatory ->Modify by Dirk 2010-11-09

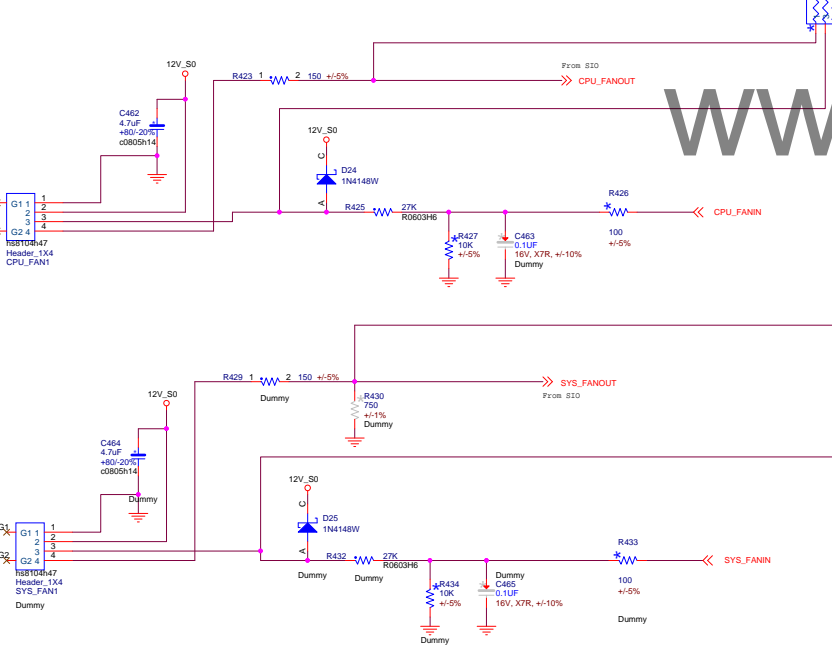
change R479 from 100K ohm to 2.2K ohm for fix APU\_VDDIO\_SUS power drop oscillatory ->Modify by Dirk 2010-11-09

POWER GOOD CIRCUIT

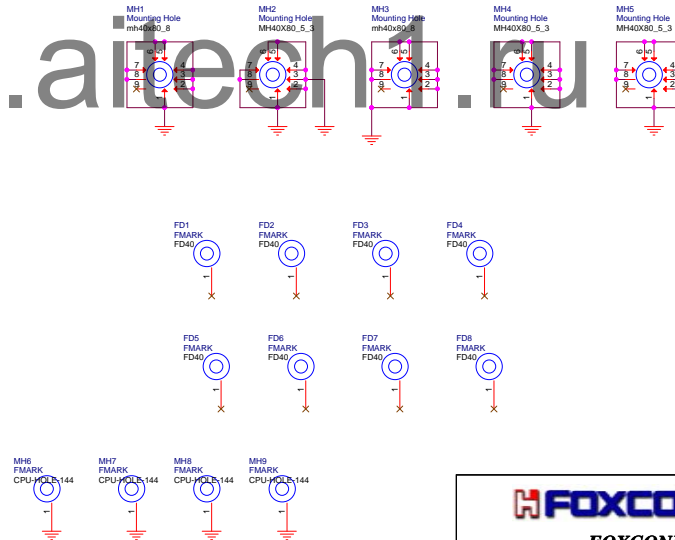


Delete CP17 and 1D05V\_PWRGD for output FCH\_PWRGD for power sequence request -->Modify by Dirk 2010-11-03

FANS

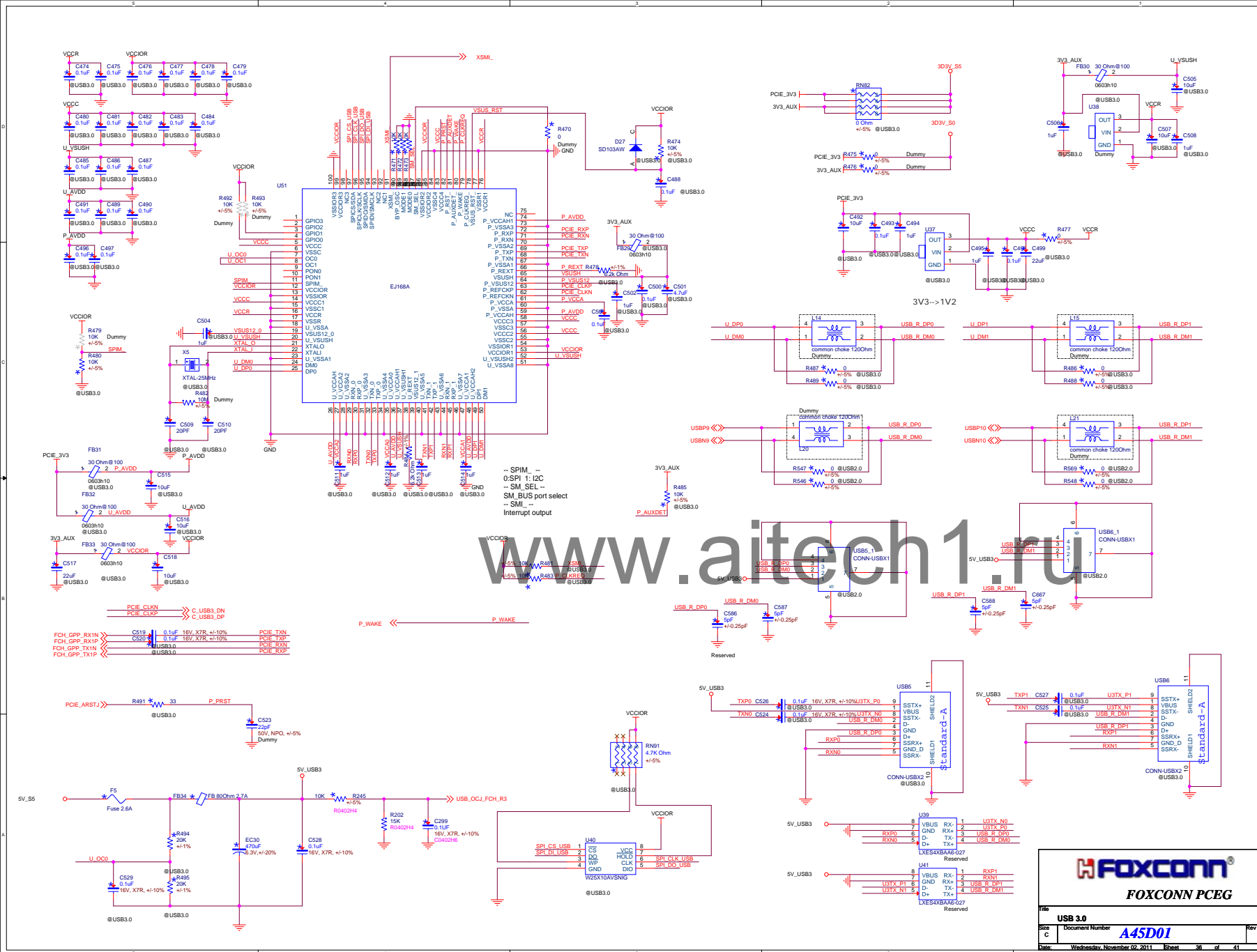


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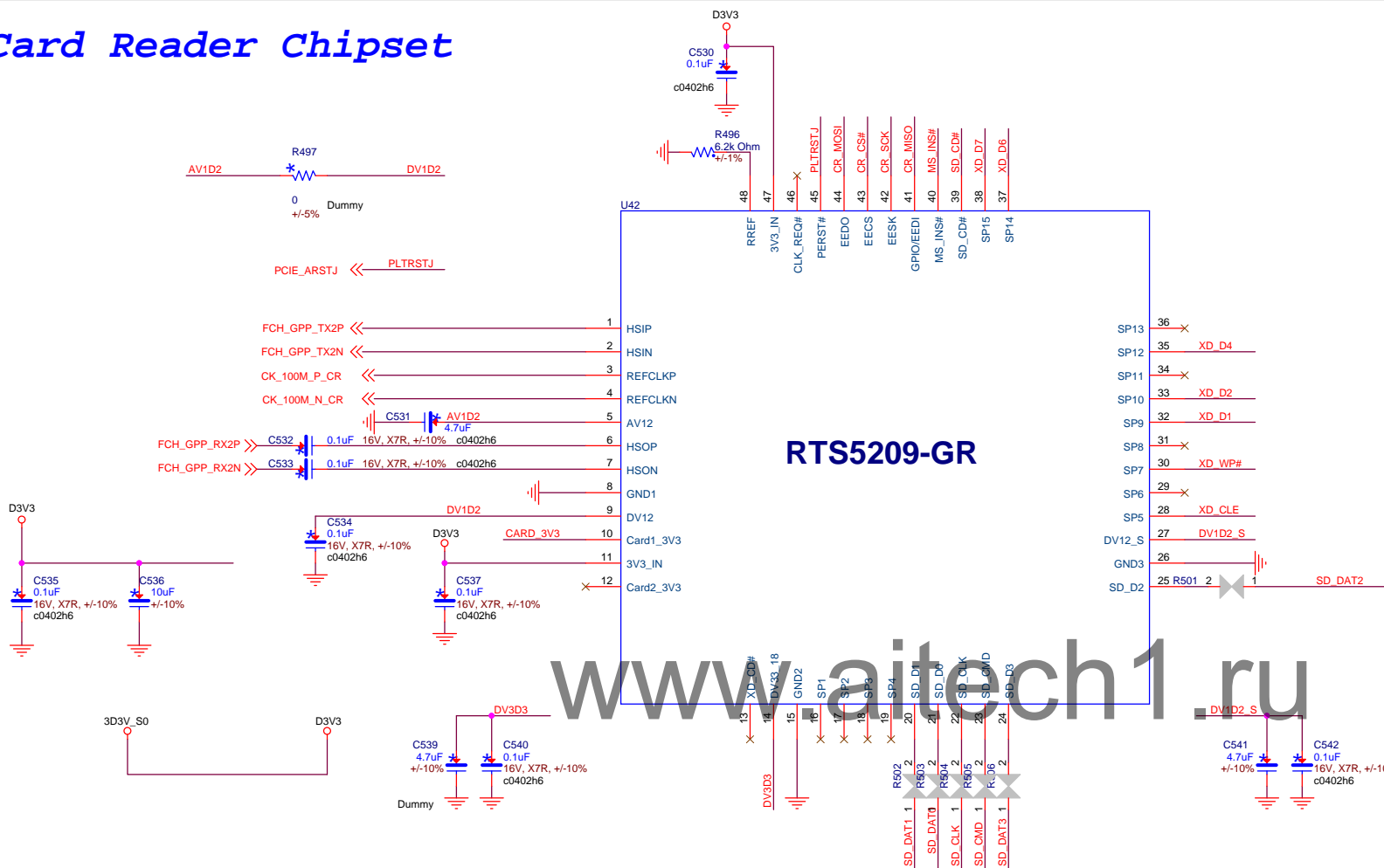


**FOXCONN**  
FOXCONN PCEG

Title		
FANS & PWRGD & ENABLES		
Size	Document Number	Rev
Custom	A45D01	
Date	Wednesday, October 26, 2011	Sheet 35 of 41

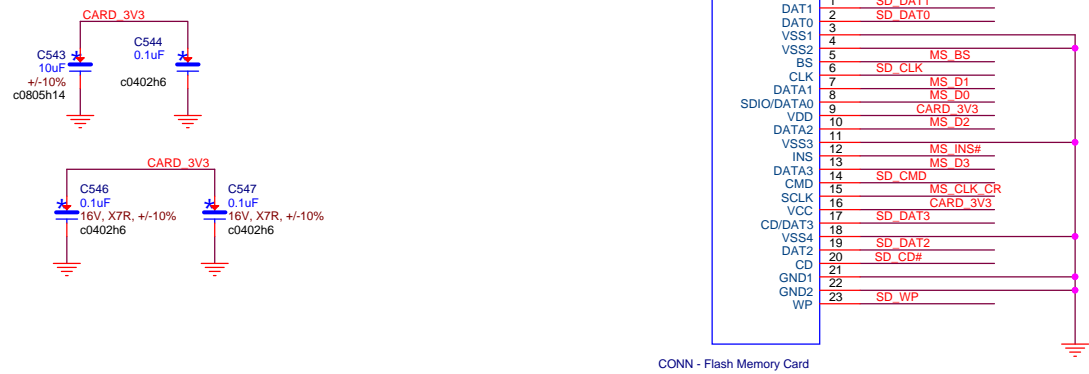


Card Reader Chipset

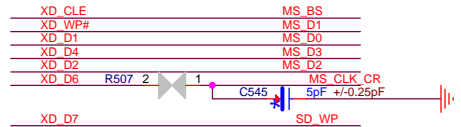



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Card Reader Connector



Share Pin





**FOXCONN PCEG**

Title

**Card Reader**

Size A3

Document Number **A45D01**

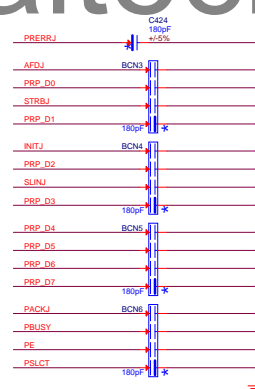
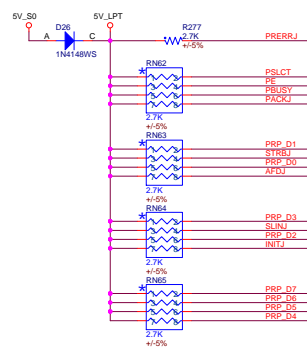
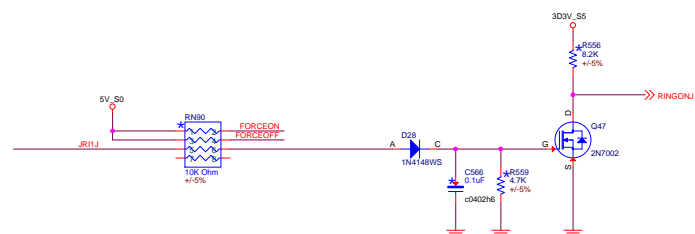
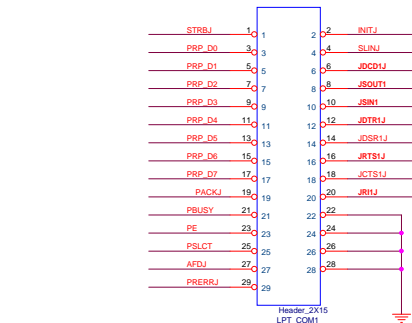
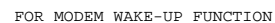
Date: Wednesday, October 26, 2011

Sheet 37 of 41

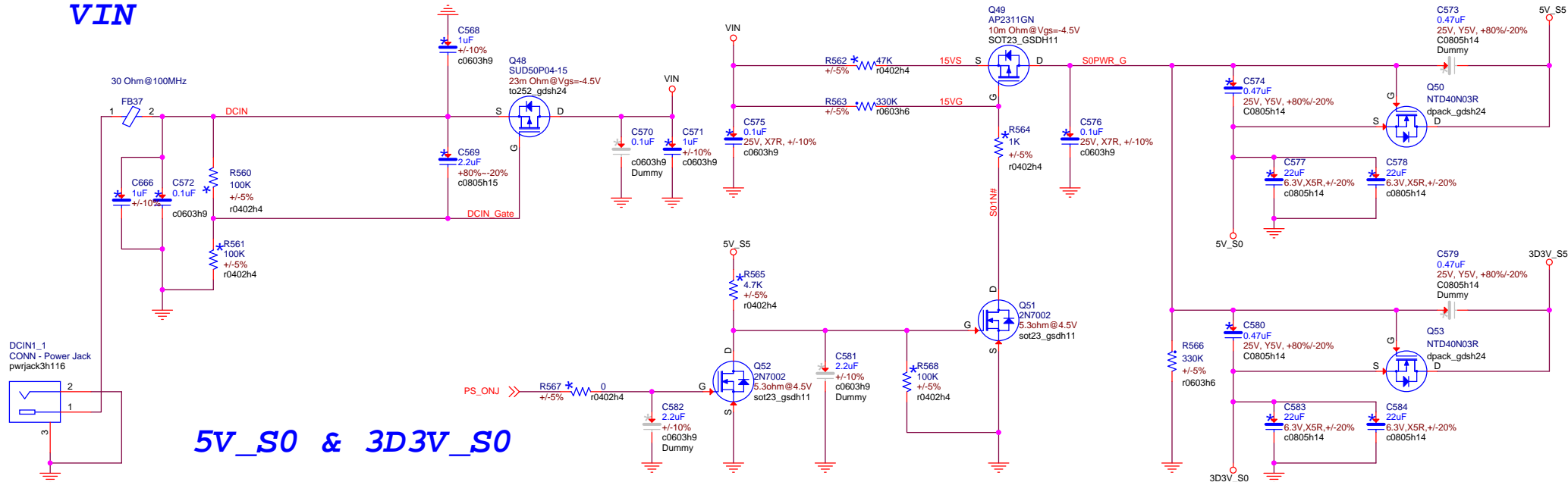
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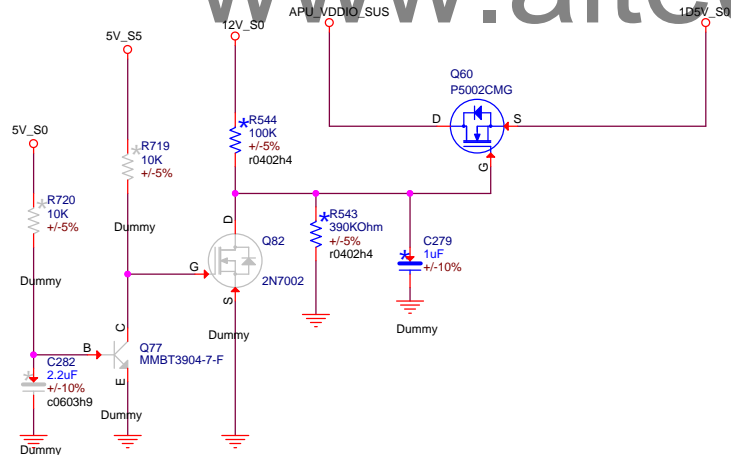


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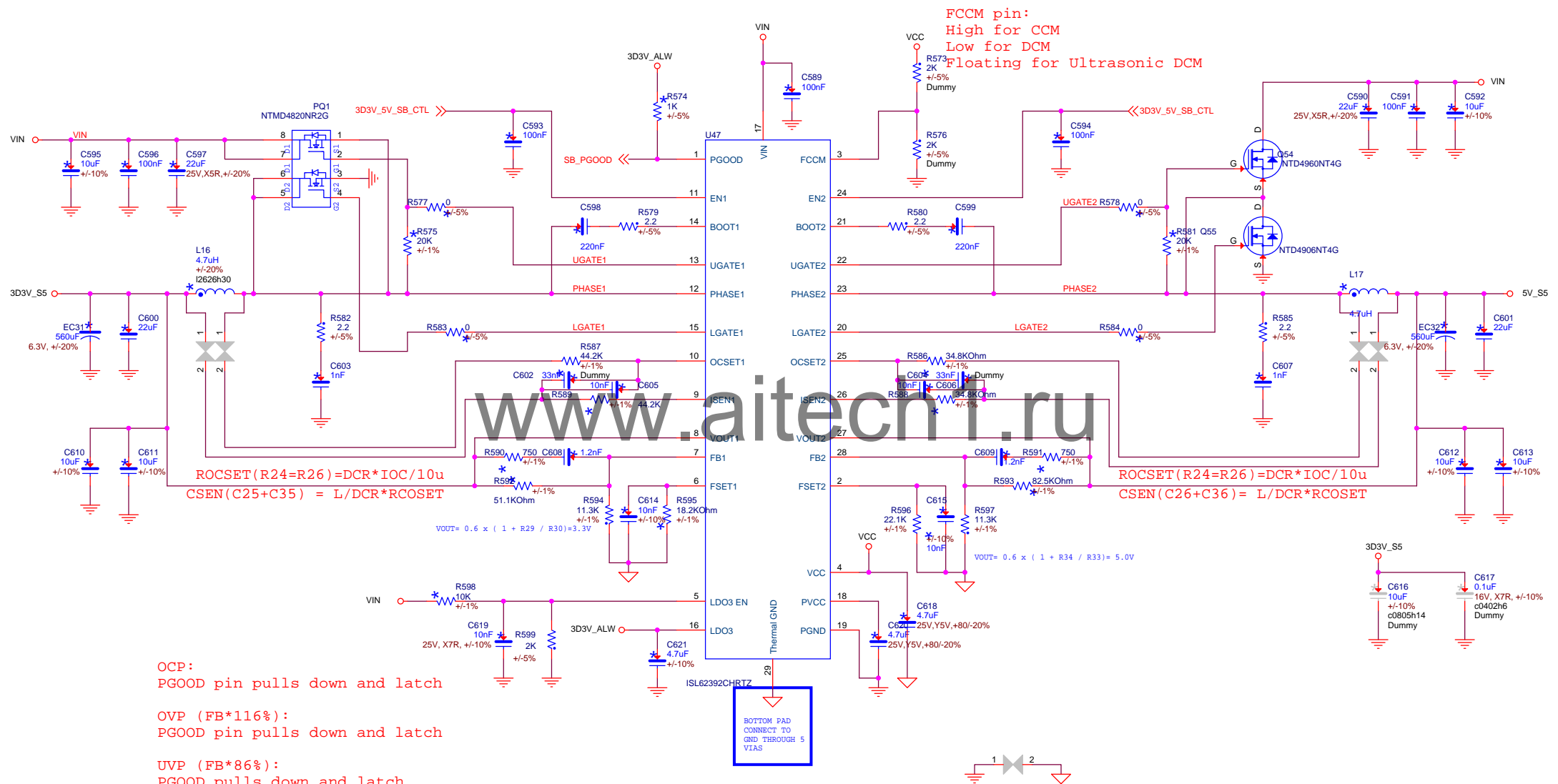


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**FOXCONN PCEG**

Title		Power_Plane/3D3V_SB	
Size	A3	Document Number	A45D01
Date:	Wednesday, October 26, 2011	Sheet	40 of 41

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OCP:  
PG0OD pin pulls down and latch

OVP (FB\*116%):  
PG0OD pin pulls down and latch

UVP (FB\*86%):  
PG0OD pulls down and latch

$$FSW = 1 / (1.5 * 10^{-10} * R_{fset})$$



**FOXCONN PCEG**

Title		ISL62392C_5V_S5/3D3V_S5	
Size	Document Number		Rev
A3	<b>A45D01</b>		
Date:	Wednesday, October 26, 2011	Sheet	41 of 41

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